Power Losses in Monolithic Buck DC-DC Converter Designed on CMOS 0.35μm Technology

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Abstract - **This paper includes investigations of power losses in monolithic buck dc-dc converter designed with Cadence on CMOS 0.35 μm process. Input voltage of the designed circuit is equal to 3.6 V and output voltage is regulated to 1.2 V. Evaluated and estimated are power dissipations in the MOS transistor, filter inductor and filter capacitor of the buck converter. Investigated and compared are losses in the off-chip filter inductors of the company Murata and on-chip filter inductors. For the extraction of the model's parameters of integrated inductors CMOS 0.35 μm process is used "Virtuoso Passive Component Designer".**

Keywords – **Monolithic buck dc-dc converter, Power losses, Cadence, CMOS 0.35 μm technology.**

I. Introduction

The market of battery operated portable electronic devices is rising very fast. The requirement to extend the battery life and the system run-time becomes stringent. The integration of the power supply regulator with electronic systems on the same chip will reduce the size and cost of the consumer product. In the other hand the tendency in microelectronics is decreasing of the integrated circuit's (IC) operating voltages. Switch mode dc-dc converter are power regulators which can achieve high efficiency. The high frequency of operation allows a reduction of the passive component size, which helps the successful integration. The use of low-cost CMOS process is another key to reduce cost and to facilitate integration on a single chip [1].

The losses in power stage of buck converter are much higher compare to the energy dissipation in the feedback control system [2]. They dominate and determine the efficiency of the system. The sources of power losses have been analyzed in order to minimize them and to increase the converter efficiency.

This paper presents the investigations results of power losses in buck converter implemented on standard CMOS 0.35-μm technology. In Section II are shown the received simulations results with Cadence. This section is divided on three parts. In Section II *A* is presented power losses in the MOS transistors of switching mode buck dc-dc converter. In Section II *B* are shown received simulations results for power dissipations in the off-chip and on-chip filter inductors in the circuit. Power losses in the filter capacitor of monolithic buck converter are presented in Section II *C*.

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II. Investigations of Power Losses in Monolithic Buck Converter

In Fig. 1 is shown the circuit of a buck converter implemented on standard CMOS 0.35-μm technology. The NMOS and PMOS transistors, which are forming the power stage, are synchronously controlled in a way that when one of the transistors is switched-on the other is switched-off. For the power losses investigation of the buck converter an input voltage of 3.6V is chosen for the converter, since this is the normal voltage for Lithium-Ion battery cell that is typically used in battery-powered devices. The output voltage V_{out} is regulated to 1.2V, which on the other hand is determined by the standard supply voltages of advanced CMOS processes.

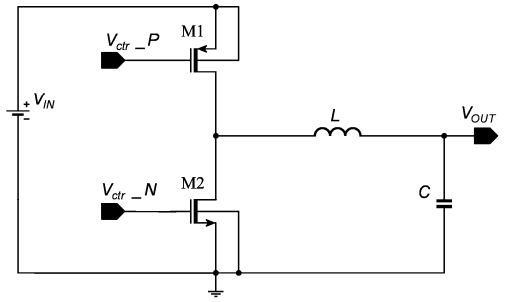

Fig. 1. Synchroneous buck converter schematic.

Power consumption in synchroneous buck converter is consisting from conduction and the switching losses. They string up respectively in the parasistic impedence and in the paraistic capacitances of the componets. In the power stage of the converter, power dissipations are in the switchnig MOS transistors, filter inductor and filter capacitance.

A. Power losses in the MOS transistors

The total power losses in the MOS transistors are a combination of conduction losses and dynamic switching losses. The dynamic power is dissipated each switching cycle during the charging and discharging of the parasitic capacitance. The average power consumption in MOS transistors is equal to [3]:

$$P_{MOS} = \frac{R_0}{W} i_{rms}^2 + E \Psi \Psi f_s \qquad (1)$$

where P_{MOS} is the total power consumed from the MOS transistors during a switching cycle, R_0 is the equivalent series resistance of the 1 μm wide MOS transistor, i_{rms} is

the rms current passing through MOS transistor, E is the unit energy consumed during a full switching cycle of MOS transistor, W is the width of the MOS transistor, f_s is the switching frequency of the buck converter.

Optimized power consumption of a buck converter is equal to:

$$P_{tot,MOS}(opt) = a\sqrt{(I^2 + \frac{\Delta i_L^{\,2}}{3})f_s} \qquad (2)$$

where a is a coefficient, Δi_L is inductor current ripple.

Power losses in the MOS transistors of buck converter implemented on CMOS 0.35-µm technology are investigated with Cadence, as a function of the switching frequency f_s and the inductor current ripple Δi_L. In Table 1 are presented received results for average output current of the converter $I_{out\ (av)}$ equal to 20 mA and Δi_L=2x$I_{out\ (av)}$.

TABLE 1. POWER LOSSES IN THE MOS TRANSISTORS OF BUCK CONVERTER FOR $I_{out\ (av)}$=20 mA

	L=10 nH	L=50 nH	L=100 nH	L=200 nH
$V_{out\ (av)}$ [V]	1.2	1.2	1.2	1.2
$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	1600	400	200	100
f_c [MHz]	80	35	25	20
P_{PMOS} [mW]	30	8.4	4.95	3.55
P_{NMOS} [mW]	12.9	4.5	3	2.5

Power losses in the MOS transistors of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=20 mA are graphically presented in Fig.2.

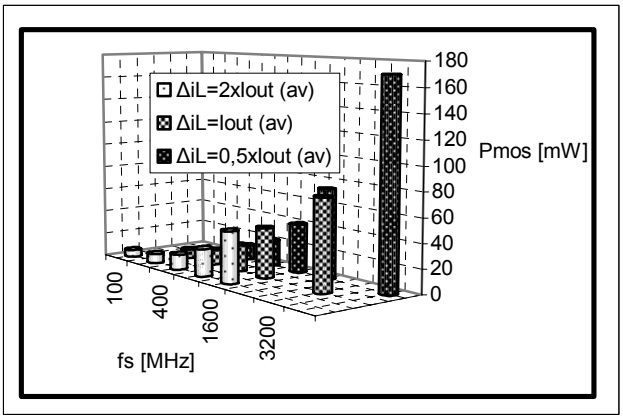

Fig. 2. Power losses in the MOS transistors of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=20 mA.

In Table 2 are presented received results for average output current of the converter $I_{out\ (av)}$ equal to 80 mA and Δi_L=$I_{out\ (av)}$.

Power losses in the MOS transistors of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=80 mA are graphically presented in Fig.3.

TABLE 2. POWER LOSSES IN THE MOS TRANSISTORS OF BUCK CONVERTER $I_{out\ (av)}$=80 mA

	L=10 nH	L=50 nH	L=100 nH	L=200 nH
$V_{out\ (av)}$ [V]	1.2	1.2	1.2	1.2
$I_{out\ (av)}$ [mA]	80	80	80	80
f_s [MHz]	800	200	100	50
f_c [MHz]	80	35	25	20
P_{PMOS} [mW]	56.58	44.5	44.8	45.36
P_{NMOS} [mW]	19.5	18.7	18.4	17.84

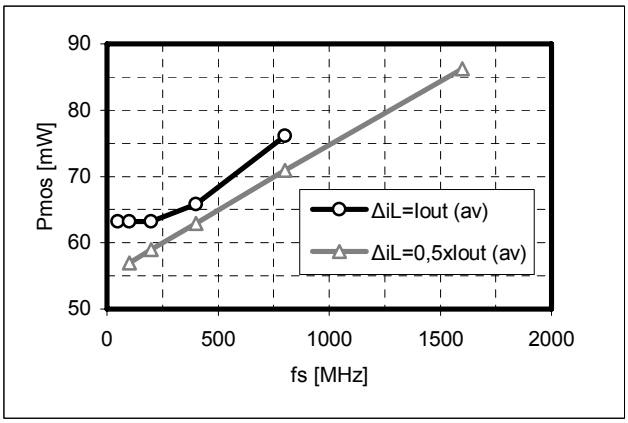

Fig. 3. Power losses in the MOS transistors of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=80 mA.

As can be seen from Fig. 2 and Fig. 3 power losses in the MOS transistors of synchroneous buck converter increased with increasing of switchnig frequency f_s and inductor current ripple Δi_L.

B. Power losses in the filter inductor

Part of the total power losses in the monolithic switching mode buck dc-dc converter are due to the series resistance and parasitic capacitance of the filter inductor. Integrated inductors have high series resistance, which grow up with increasing of the inductor's value. This lead to the low quality factor Q of these components [4]. Integration of a spiral inductor with sufficient inductance is not feasible, because they occupy huge silicon area and have low Q factor. The total power dissipated in filter inductor, assuming that the inductor parasitic impedance scale linearly with the inductance is equal to [3]:

$$P_{ind} = b\left(\frac{I^2}{\Delta i_L f_s} + \frac{\Delta i_L}{3 f_s} + \frac{C_{L0} V_{DD1}^2}{R_{L0} \Delta i_L}\right) \qquad (3)$$

where b is a coefficient depending from the parasitic capacitance and parasitic series resistance of the filter inductor, C_{L0} and R_{L0} are respectively the parasitic stray capacitance and parasitic series resistance per 1 nH inductance, V_{DD1} is power supply.

Power losses in the filter inductor of the synchroneous buck converter designed on CMOS 0.35-µm technology are analyzed with Cadence, as a function of switchnig frequency f_s and inductor current ripple Δi_L. Integrated

passive inductors and capacitors occupied huge silicon area, which make more expensive the electronic devices. In order to be evaluated and compared the power losses in off-chip and on-chip filter inductor of monolithic buck dc-dc converter are made many investigations.

The received results of power losses in the off-chip filter inductor of buck dc-dc converter are presented below. For the simulations with Cadence on CMOS 0.35-µm technology are used inductor's models of the company Murata [5]. In Table 3 are presented power losses in the off-chip filter inductor P_{ind} as a function of switchnig frequency f_s and inductor current ripple Δi_L. Average output current of the buck converter $I_{out\ (av)}$ equal to 20 mA and $\Delta i_L = I_{out\ (av)}$.

TABLE 3. POWER LOSSES IN THE OFF-CHIP FILTER INDUCTORS OF BUCK CONVERTER $I_{out\ (av)}$=20 mA

	L=10 nH	L=100 nH	L=200 nH	L=470 nH
$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	2500	750	500	350
$\Delta i_L/I_{out\ (av)}$	1	1	1	1
P_{ind} [mW]	0.056	0.333	1.02	2.88

Power losses in the off-chip filter inductor P_{ind} of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=20 mA are graphically presented in Fig.4. For simulations the inductor's models of the company Murata are used.

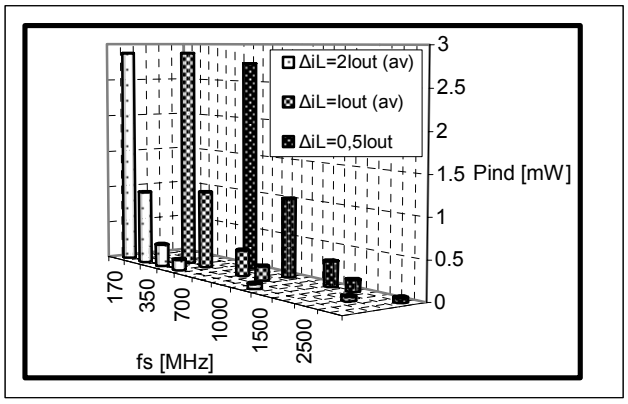

Fig. 4. Power losses in the off-chip filter inductor of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=20 mA.

The dependence of the power dissipation in integrated filter inductors of CMOS 0.35-µm technology are investigated and evaluated. Standard monolithic inductances are not optimized for the specific applications. In the other hand theirs number of values are limited. That's way is necessary to be designed integrated inductance with desired value and geometry. One of the Cadence tools named "Virtuoso Passive Component Designer" is used for the extraction of inductor's model parameters [6]. The values of the extracted parameters are used for simulations.

The received results of power losses in the on-chip filter inductor of buck dc-dc converter are presented below. Investigations are made for average output current of the buck converter $I_{out\ (av)}$ equal to 20 mA. In Table 4 are presented power losses in the on-chip filter inductor P_{ind} as a function of switchnig frequency f_s and inductor current ripple Δi_L, for $\Delta i_L = I_{out\ (av)}$.

TABLE 4. POWER LOSSES IN THE ON-CHIP FILTER INDUCTORS OF BUCK CONVERTER $I_{out\ (av)}$=20 mA

	L=10 nH	L=14,1 nH	L=51 nH	L=82 nH
$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	2500	2000	1000	750
$\Delta i_L/I_{out\ (av)}$	1	1	1	1
P_{ind} [mW]	15.37	15.74	23.6	32.78

Power losses in the on-chip filter inductor P_{ind} of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=20 mA are graphically presented in Fig. 5.

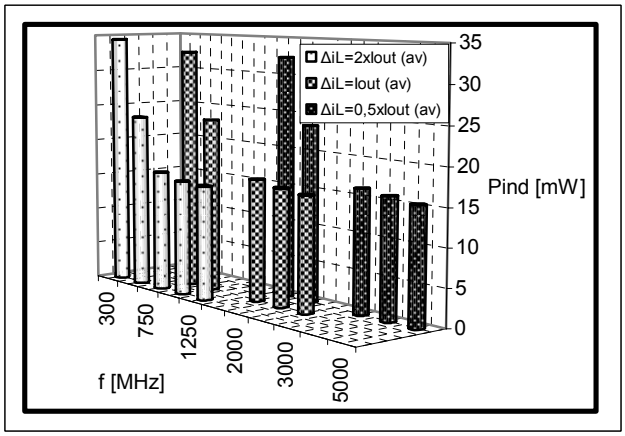

Fig. 5. Power losses in the on-chip filter inductor of buck converter implemented on CMOS 0.35-µm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=20 mA.

As can be seen from Fig. 4 and Fig. 5 power losses in the filter inductor of buck dc-dc converter goes down with increasing of switchnig frequency f_s and inductor current ripple Δi_L. When off-chip filter inductors of the company Murata are used, power dissipation is around 10 times lower compare to the losses in integrated inductors of CMOS 0.35-µm process (Fig. 4, Fig. 5). The reason is the high series resistance and low Q factor of the monolithic inductors.

Power losses in the switching mode buck dc-dc converter are mainly in the filter inductor at low f_s and Δi_L. With increasing of switchnig frequency f_s and inductor current ripple Δi_L, the inductance value decreasing and power dissipation in the parasitic components is lower. In the other hand with increasing of switchnig frequency f_s, power losses in the MOS transistors goes up. In a particular area of change of the f_s and Δi_L, power losses in the filter inductor dominate in the buck dc-dc converter. In this region with increasing of switchnig frequency and inductor current ripple, total power losses in the converter decreased. After reaching of the maximum efficiency of buck dc-dc converter, power losses in the MOS transistors are starting to dominate. Upon further increase of f_s и Δi_L the efficiency of the converter decreased. There is a

optimum values of the switchnig frequency f_s and inductor current ripple Δi_L at which efficiency of the buck dc-dc converter has a maximum.

C. Power losses in the filter capacitor

Power losses in the filter capacitor C of the buck dc-dc converter are due to the effective series resistance of the capacitance R_C. Assuming that monolithic capacitor is implemented utilizing the gate oxide capacitance of a MOSFET transistor, the total power dissipation of filter capacitor is equal to [3]:

$$P_{cap} = d \Psi f_s \Psi \Delta i_L \quad (4)$$

where d is a coefficient depending from the technology, effective series resistance of the filter capacitor for MOSFET transistor with channel width equal to 1 μm, gait oxide capacitance, channel length of the MOSFET transistor.

Power losses in the filter capacitor of buck dc-dc converter designed on CMOS 0.35-μm technology, are investigated with Cadence. Their function from switchnig frequency f_s and inductor current ripple Δi_L is evaluated. In Table 5 are presented received results for power losses in the filter capacitor P_{cap}, for average output current of the buck converter $I_{out\ (av)}$ equal to 20 mA and $\Delta i_L = I_{out\ (av)}$.

TABLE 5. POWER LOSSES IN THE ON-CHIP FILTER INDUCTORS OF BUCK CONVERTER $\Delta i_L = I_{out\ (av)}$

$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	2500	2000	1000	750
$\Delta i_L / I_{out\ (av)}$	1	1	1	1
P_{cap} [mW]	0.087	0.083	0.076	0.070

In Table 6 are presented received results for power losses in the filter capacitor P_{cap}, for average output current of the buck converter $I_{out\ (av)}$ equal to 20 mA and $\Delta i_L = 2 \times I_{out\ (av)}$.

TABLE 6. POWER LOSSES IN THE ON-CHIP FILTER INDUCTORS OF BUCK CONVERTER $\Delta i_L = 2 \times I_{out\ (av)}$

$I_{out\ (av)}$ [mA]	20	20	20	20
f_s [MHz]	1250	1000	500	300
$\Delta i_L / I_{out\ (av)}$	2	2	2	2
P_{cap} [mW]	0.162	0.158	0.147	0.1416

Power losses in the filter capacitor P_{cap} of buck converter implemented on CMOS 0.35-μm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=20 mA are graphically presented in Fig. 6.

As can be seen from the Fig. 6 power losses in the filter capacitor of the buck dc-dc converter designed on CMOS 0.35-μm technology are considerably smaller than power dissipation in the MOS transistors and filter inductor for the entire range of variation of f_s и Δi_L. They are between 0.5 % and 5 % from the power losses respectively in the off-chip and on-chip filter inductors (Fig. 4, Fig. 5).

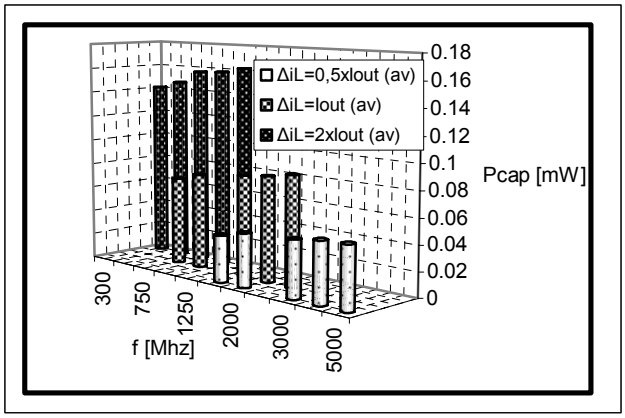

Fig. 6. Power losses in the filter capacitor of buck converter implemented on CMOS 0.35-μm technology as a function of f_s and Δi_L, for $I_{out\ (av)}$=20 mA.

III. CONCLUSION

The power losses in the monolithic buck dc-dc converter designed on CMOS 0.35 μm technology has been investigated and evaluated. The received results shows that by increasing of switchnig frequency f_s of the circuit power dissipations in the MOS transistors and filter capacitors go up and losses in the filter inductor decreased. Similarly power losses in the MOS transistors and filter capacitors increased by increasing of inductor current ripple Δi_L. By increasing of the Δi_L requirements for the inductor's value decreased for fixed switchnig frequency f_s. This reduces the parasitic impedance of the filter inductor and the related power loss. A higher value of the Δi_L leads to the increasing of rms current through the inductor which causes to the bigger conduction losses in the inductor.

IV. ACKNOWLEDGMENTS

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